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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,160	02/05/2002	Ronald L. Schlupp	M-12381 US	1248

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EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	2

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,160	SCHLUPP ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al (US 6,057,207)

Lin discloses a method of planarizing a semiconductor substrate. This method comprises the steps of:

providing a trench isolation structure 10, the structure 10 includes a multi-layer film stack on a plurality of device regions 12A and 12B on the substrate 10, the device region 12A are separated from the device region 12B by one trench 30, the trench is filled with oxide layer 40 (col 4, lines 66-67, fig. 1)

performing a first CMP (chemical mechanical polishing) to polish oxide layer 40, the polish stops at the barrier layer 44 of the multi-film stack on the substrate 10 (col 47-49, fig.4), which reads on performing a first polish to polish the oxide to the level of a first polish stop layer of the multi-stack

performing a second CMP (chemical mechanical polishing) to polish oxide layer 40 to the level of second barrier layer 24/stop layer of the multi-film stack (col 7, lines 39-45, fig. 7)

The limitation of claims 2, 4 has been discussed above

Regarding claim 3, fig. 1 of Lin shows that trenches 30 are etched through the multi-layer stack film into portions of the substrate 10.

Regarding claim 5, Lin discloses forming a first oxide liner and second oxide 20, the oxide liner/first oxide is disposed between first barrier layer 44/polish stop layer and second barrier layer 24/stop layer, the second oxide layer 20 is formed between layer 24/second stop layer and substrate 10 (col 4, lines 39-65, col 5, lines 20-21; fig. 2)

Regarding claim 6, fig. 7 shows that oxide liner/first oxide is removed after the first CPM.

Regarding claim 7, Lin discloses that first barrier layer 44/polish stop layer and second barrier 24/stop layer are silicon nitride (col 5, lines 49-50, col 6, lines 41-42)

Regarding claims 8, 9, Lin discloses that the first barrier layer 44/polish stop layer and second barrier 24/stop layer are removed after the polishing steps (fig. 8)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-15, 19-20, 24-30, 33-37, 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin e al (US 6,057,207) in view of Parat et al (US 6,194,784)

Lin discloses a method of planarizing a semiconductor substrate. This method comprises the steps of:

forming a multi-layer film stack comprises a second oxide layer 20 disposed above the substrate 10, a second nitride layer 24 disposed above layer layer 20/second oxide layer, an oxide liner/first oxide layer disposed above second nitride layer 24, a first nitride layer 44 disposed above the oxide liner, the multi-layer film stack disposed on first device region 12A separated from second device region12B by trench 30 (col 4, lines 39-65, col 5, lines 20-21; fig. 2). The trenches are formed by etching (col 1, lines 62-63)

depositing oxide 40 to fill the trenches (col 2, lines 51-54)

polishing down the layer 40/trench oxide (col 50-52)

Unlike the instant claimed invention as per claims 10, 29, Lin fails to disclose depositing a trench oxide/an oxide to fill the trench to cover the first nitride.

However, Parat discloses a process for forming a gate stack comprises the step of depositing trench oxide layer 221 to cover nitride layer 238/first nitride (col 6, lines 50-52)

Since both Lin and Parat are directed to method of forming gate having stacked layer, one skilled in the art would have found it obvious to modify Lin method by adding the step of depositing trench oxide layer to cover nitride layer as per Parat because according to Parat, following the encapsulation of the stack in silicon nitride etch stop layer, an upper insulative or dielectric layer is preferably formed over/to cover the semiconductor device to create a upper layer (col 6, lines 50-56)

Regarding claims 11, 30, Lin discloses performing a first CMP (chemical mechanical polishing) to polish oxide layer 40 exposing the barrier layer 44/first nitride layer (col 47-49, fig.4)

Regarding claims 12, 37, Lin discloses performing a second CMP (chemical mechanical polishing) to polish oxide layer 40 exposing the second barrier layer 24/second nitride layer (col 7, lines 39-45, fig. 7)

Regarding claims 13-15, 35, Fig. 8 of Lin shows that layer 44/first nitride layer, the liner oxide layer and layer 24/second nitride layer are removed from the semiconductor structure.

Regarding claims 19-20, Lin discloses that the oxide liner/first oxide layer having a thickness of between 200-400 Angstroms (col 5, lines 22-24), which overlaps the claimed range of 100-400 Angstroms.

Regarding claims 24, 27, fig. 2 of Lin shows that first device region 12A is larger than second device region 12B

Regarding claims 25, 26, Fig. 8 of Lin shows that after the first CMP step, the height of the first device region 12A is approximately equal to the height difference between the top of trench oxide 40 and the first edge of first device region 12A, the height of the second device region 12B is approximately equal to the height difference between the top of trench oxide 40 and the first edge of second device region 12B. Lin also discloses that the height difference between the top surface of trench oxide and the top surface of the active regions 12A 12B in a range of 300-700 Angstroms.

Regarding claims 28, 42, Lin discloses forming an oxide liner layer/oxidation layer prior to forming trench oxide 40 (col 5, lines 20-22)

Regarding claims 33- 34, 40-41, Lin discloses using phosphoric acid to remove nitride layer (col 7, lines 47-48)

Regarding claims 35-36, Lin discloses removing the oxide layer/insulating layer using dry etch (col 7, lines 4-7)

5. Claims 16-17, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US 6,057,207) in view of Parat et al (US 6,194,784) and further in view of Lyons et al (US 5,930,645)

Lin as modified by Parat has been described above in paragraph 4. Unlike the instant claimed inventions as per claims 16-17, 19-22, Lin and Parat do to disclose the specific thickness of the layers.

However, Lyons, in a method of forming trench isolation, teaches that the thickness of a layer depending on the variables of the polishing process (col 6, lines 21-23)

Thus, Lyons serves as evidence that the thickness of a layer is a "result effective variable". It has been held that the discovery of an optimum value for result effective variable is within the purview of routine experimentation by the person of ordinary skilled in the art. In re Boesch, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980)

6. Claims 18, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US 6,057,207) in view of Parat et al (US 6,194,784) and further in view of Iyer (US 6,194,305)

Lin as modified by Parat has been described above in paragraph 4. Unlike the instant claimed inventions as per claims 18, 23, Lin and Parat do to disclose forming the nitride layer by PECVD.

However, Iyer discloses a method of planarization comprises the step of forming silicon nitride by PECVD (col 4, lines 10-15)

One skilled in the art would have found it obvious to modify Lin and Parat by forming the nitride layer by PECVD as per Iyer because Iyer states that PECVD is a known process to provide conformal coating of delicate high aspect ratio feature and so are preferably to other methods of thin film formation (col 4, lines 13-17)

7. Claims 31-32, 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US 6,057,207) in view of Parat et al (US 6,194,784) and further in view of Satoh (US 6,245,642)

Lin as modified by Parat has been described above in paragraph 4. Unlike the instant claimed inventions as per claims 31-32, 38-39, Lin and Parat do to disclose using a slurry includes cerium in the step of polishing the oxide expose the nitride layer.

However, Satoh discloses a process for planarizing semiconductor device comprises the step of polishing the silicon oxide layer using a slurry includes cerium (col 4, lines 29-38)

Since Lin discloses the step of polishing an oxide layer exposing the nitride layer, one skilled in the art would have found it obvious to modify Lin and Parat by polishing the oxide layer using a slurry includes cerium as per Satoh because Satoh teaches that by using a slurry includes cerium the oxide film can be selectively polished while the polishing of the silicon oxide film is suppressed (col 4, lines 39-42)

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
May 9, 2003